Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims of this application:

Listing of Claims:

1-5.   (Canceled).

6.   (New) A Magnetic Random Access Memory (MRAM) device comprising:

an array of magnetic memory cells arranged in intersecting rows and columns, wherein each of the magnetic memory cells comprises a cell resistance;

a plurality of magnetic memory cell selection devices, each of which is coupled to a respective one of the magnetic memory cells in the array to enable selective access to any of the magnetic memory cells during a write operation, wherein each of the selection devices comprises a reverse bias resistance,

wherein a number of the rows and columns is increased by increasing the reverse bias resistance.

7.   (New) The MRAM according to Claim 6 wherein the number of the rows and columns included in the device is limited according to the relation:

$$\eta = \sqrt{\frac{R_m * \varepsilon (2 + K_{DR})}{R_r (1-\varepsilon)}}$$

where R_m comprises a resistance of one of the magnetic memory cells, ε comprises a maximum current non-uniformity of the array during a write operation, K_{DR} depends on the reverse bias resistance of one of the magnetic memory cell selection devices, and R_r comprises a resistance of a row or column of the magnetic memory cells.

8. (New) The MRAM according to Claim 7 wherein the maximum current non-uniformity of the array comprises less than about 15 percent.

9. (New) The MRAM according to Claim 8 wherein the maximum current non-uniformity of the array comprises a difference between a minimum current and a maximum current for a selected magnetic memory cell during the write operation as a percentage of a nominal current for the selected magnetic memory cell during the write operation.

10. (New) The MRAM according to Claim 6 wherein the magnetic memory cell selection devices comprises diodes or transistors.

11. (New) A method of sizing a MRAM comprising:

providing an MRAM array comprising an array of magnetic memory cells arranged in intersecting rows and columns, wherein each of the magnetic memory cells comprises a cell resistance and a plurality of magnetic memory cell selection devices, each of which is coupled to a respective one of the magnetic memory cells in the array to enable selective access to any of the magnetic memory cells during a write operation, wherein each of the selection devices comprises a reverse bias resistance;

determining a maximum current non-uniformity for the MRAM array to be provided by the array during a write operation; and

limiting a maximum number of rows and columns for inclusion in the device by increasing the reverse bias of the selection devices;

12. The method according to Claim 11 wherein the maximum number of rows and columns for inclusion in the device is limited according to the relation:

$$\eta = \sqrt{\frac{R_m * \varepsilon \left(2 + K_{DR}\right)}{R_r \left(1 - \varepsilon\right)}}$$

where R_m comprises a resistance of one of the magnetic memory cells, ε comprises a maximum current non-uniformity of the array during a write operation, K_{DR} depends on the

reverse bias resistance of one of the magnetic memory cell selection devices, and R_r comprises a resistance of a row or column of the magnetic memory cells

13. (New) The method according to Claim 12 wherein the maximum current non-uniformity of the array comprises less than about 15 percent.

14. (New) The method according to Claim 13 wherein the maximum current non-uniformity of the array comprises a difference between a minimum current and a maximum current for a selected magnetic memory cell during the write operation as a percentage of a nominal current for the selected magnetic memory cell during the write operation.

15. (New) The method according to Claim 11 wherein the magnetic memory cell selection devices comprises diodes or transistors.

16. (New) The method according to Claim 12 wherein limiting the maximum number of rows and/or columns for inclusion in the device according the relation further comprises:

eliminating an excess number of the row and/or columns form the array based on the relation during manufacture of the MRAM device.